

Hex inverter

74HC04; 74HCT04

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT04 provide six inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 6.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC04	HCT04	
t_{PHL}/t_{PLH}	propagation delay nA to nY	$C_L = 15$ pF; $V_{CC} = 5$ V	7	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

- For 74HC04: the condition is $V_I = \text{GND to } V_{CC}$.

For 74HCT04: the condition is $V_I = \text{GND to } V_{CC} - 1.5$ V.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	H
H	L

Note

- H = HIGH voltage level;
L = LOW voltage level.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC04N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT04N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC04D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT04D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC04DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT04DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC04PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT04PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC04BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT04BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V _{CC}	supply voltage

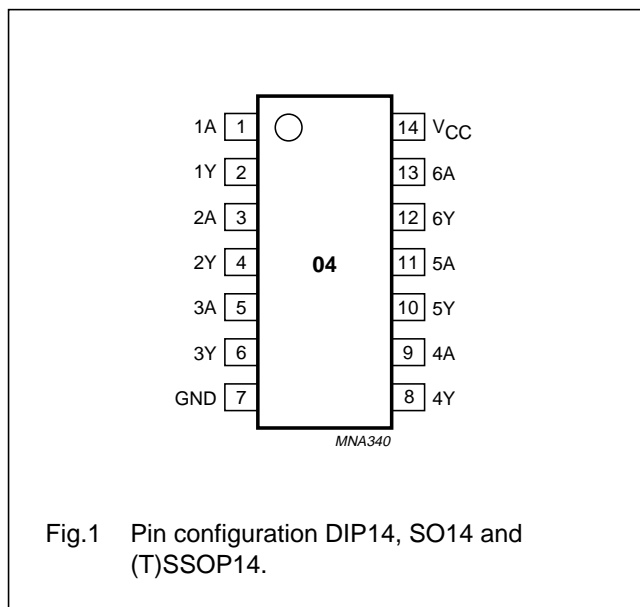


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC04			74HCT04			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0$ V	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5$ V	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0$ V	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	–	±20	mA
I_O	output source or sink current	-0.5 V < V_O < $V_{CC} + 0.5$ V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	DIP14 package	$T_{amb} = -40$ to $+125$ °C; note 1	–	750	mW
	other packages	$T_{amb} = -40$ to $+125$ °C; note 2	–	500	mW

Notes

- For DIP14 packages: above 70 °C derate linearly with 12 mW/K.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.