

Features

- Fast Read Access Time – 70 ns
- 5-volt Only Reprogramming
- Sector Program Operation
 - Single Cycle Reprogram (Erase and Program)
 - 512 Sectors (128 Bytes/Sector)
 - Internal Address and Data Latches for 128 Bytes
- Internal Program Control and Timer
- Hardware and Software Data Protection
- Fast Sector Program Cycle Time – 10 ms
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Low Power Dissipation
 - 50 mA Active Current
 - 300 μA CMOS Standby Current
- Typical Endurance > 10,000 Cycles
- Single 5V \pm 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT29C512 is a 5-volt only in-system Flash programmable and erasable read only memory (PEROM). Its 512K of memory is organized as 65,536 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 70 ns with power dissipation of just 275 mW over the industrial temperature range. When the device is deselected, the CMOS standby current is less than 300 μA . The device endurance is such that any sector can typically be written to in excess of 10,000 times.

To allow for simple in-system reprogrammability, the AT29C512 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT29C512 is performed on a sector basis; 128 bytes of data are loaded into the device and then simultaneously programmed.

During a reprogram cycle, the address locations and 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the sector and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{\text{DATA}}$ polling of I/O7. Once the end of a program cycle has been detected, a new access for a read or program can begin.



**512K (64K x 8)
5-volt Only
Flash Memory**

AT29C512



4.7 $\overline{\text{DATA}}$ Polling

The AT29C512 features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

4.8 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling the AT29C512 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.9 Optional Chip Erase Mode

The entire device can be erased by using a 6-byte software code. Please see Software Chip Erase application note for details.

5. Absolute Maximum Ratings*

Temperature Under Bias.....	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{CC} + 0.6V$
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. DC and AC Operating Range

		AT29C512-70	AT29C512-90
Operating Temperature (Case)	Industrial	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		5V ± 5%	5V ± 10%

7. Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	Ai	I/O
Read	V _{IL}	V _{IL}	V _{IH}	Ai	D _{OUT}
Program ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	Ai	D _{IN}
5V Chip Erase	V _{IL}	V _{IH}	V _{IL}	Ai	
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	X	High Z
Program Inhibit	X	X	V _{IH}		
Program Inhibit	X	V _{IL}	X		
Output Disable	X	V _{IH}	X		High Z
Product Identification					
Hardware	V _{IL}	V _{IL}	V _{IH}	A1 - A15 = V _{IL} , A9 = V _H , ⁽³⁾ A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A1-A15 = V _{IL} , A9 = V _H , ⁽³⁾ A0 = V _{IH}	Device Code ⁽⁴⁾
Software ⁽⁵⁾				A0 = V _{IL}	Manufacturer Code ⁽⁴⁾
				A0 = V _{IH}	Device Code ⁽⁴⁾

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC Programming Waveforms.
 3. V_H = 12.0V ± 0.5V.
 4. Manufacturer Code: 1F, Device Code: 5D.
 5. See details under Software Product Identification Entry/Exit.

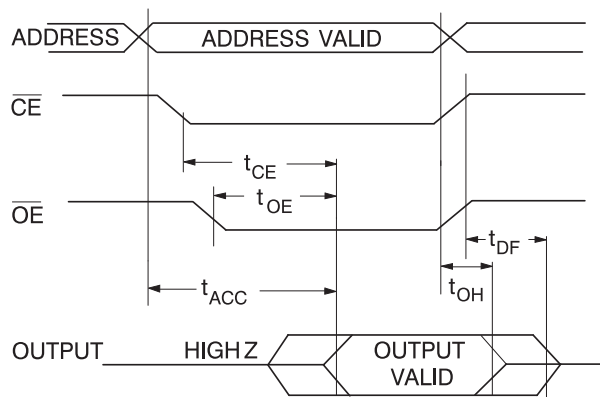
8. DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC}		300	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC}		3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		50	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4		V
V _{OH2}	Output High Voltage CMOS	I _{OH} = -100 μA; V _{CC} = 4.5V	4.2		V

9. AC Read Characteristics

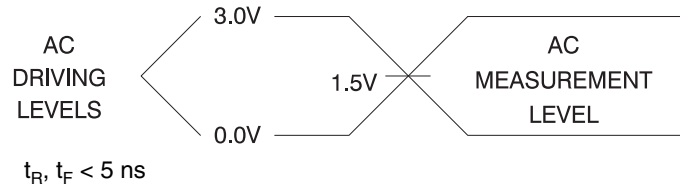
Symbol	Parameter	AT29C512-70		AT29C512-90		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90	ns
$t_{CE}^{(1)}$	\overline{CE} to Output Delay		70		90	ns
$t_{OE}^{(2)}$	\overline{OE} to Output Delay	0	35	0	40	ns
$t_{DF}^{(3)(4)}$	\overline{CE} or \overline{OE} to Output Float	0	10	0	25	ns
t_{OH}	Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first	0		0		ns

10. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

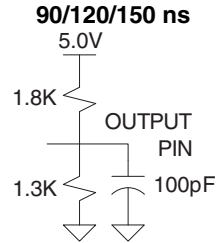
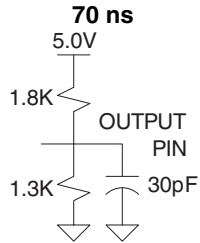


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

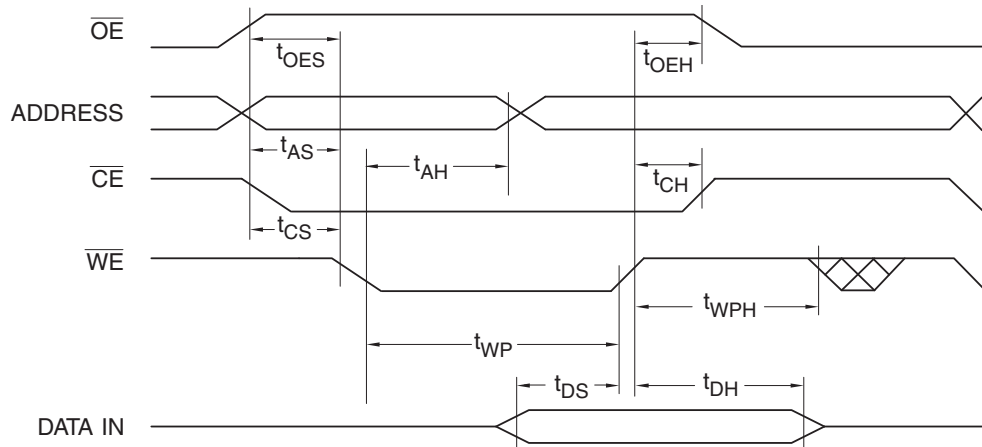
Note: 1. This parameter is characterized and is not 100% tested.

14. AC Byte Load Characteristics

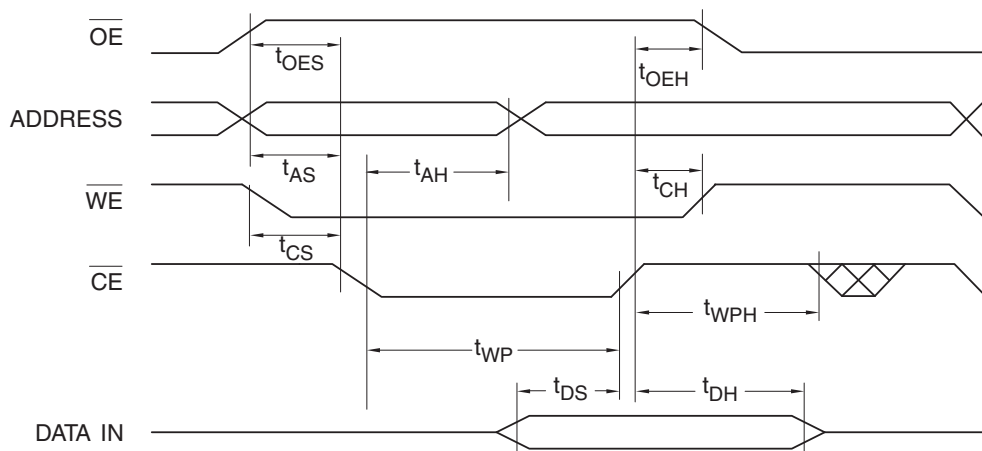
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, \overline{OE} Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (\overline{WE} or \overline{CE})	90		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}, t_{OEH}	Data, \overline{OE} Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

15. AC Byte Load Waveforms

15.1 \overline{WE} Controlled



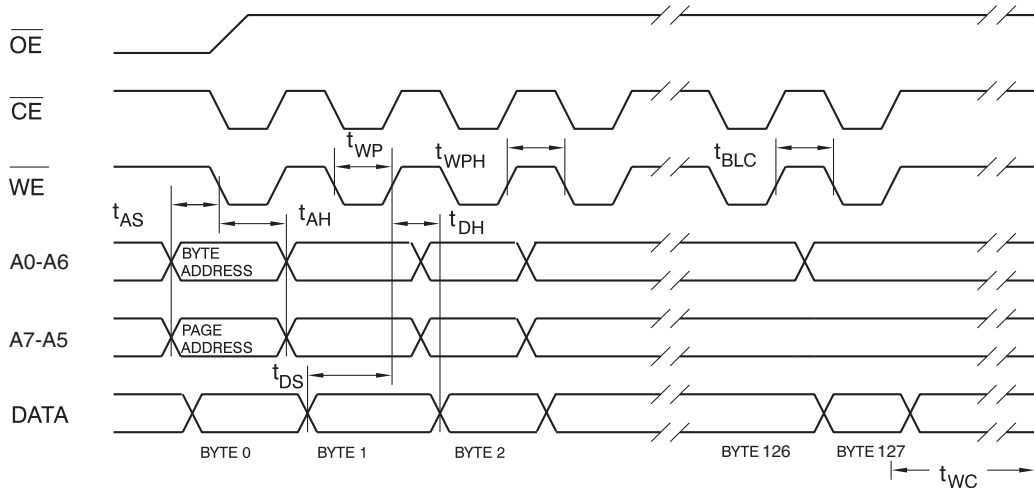
15.2 \overline{CE} Controlled



16. Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	35		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	90		ns
t_{BLC}	Byte Load Cycle Time		150	μ s
t_{WPH}	Write Pulse Width High	100		ns

17. Program Cycle Waveforms ⁽¹⁾⁽²⁾⁽³⁾



- Notes:
1. A7 through A15 must specify the sector address during each high-to-low transition of \overline{WE} (or \overline{CE}).
 2. \overline{OE} must be high when \overline{WE} and \overline{CE} are both low.
 3. All bytes that are not loaded within the sector being programmed will be indeterminate.

28. Ordering Information

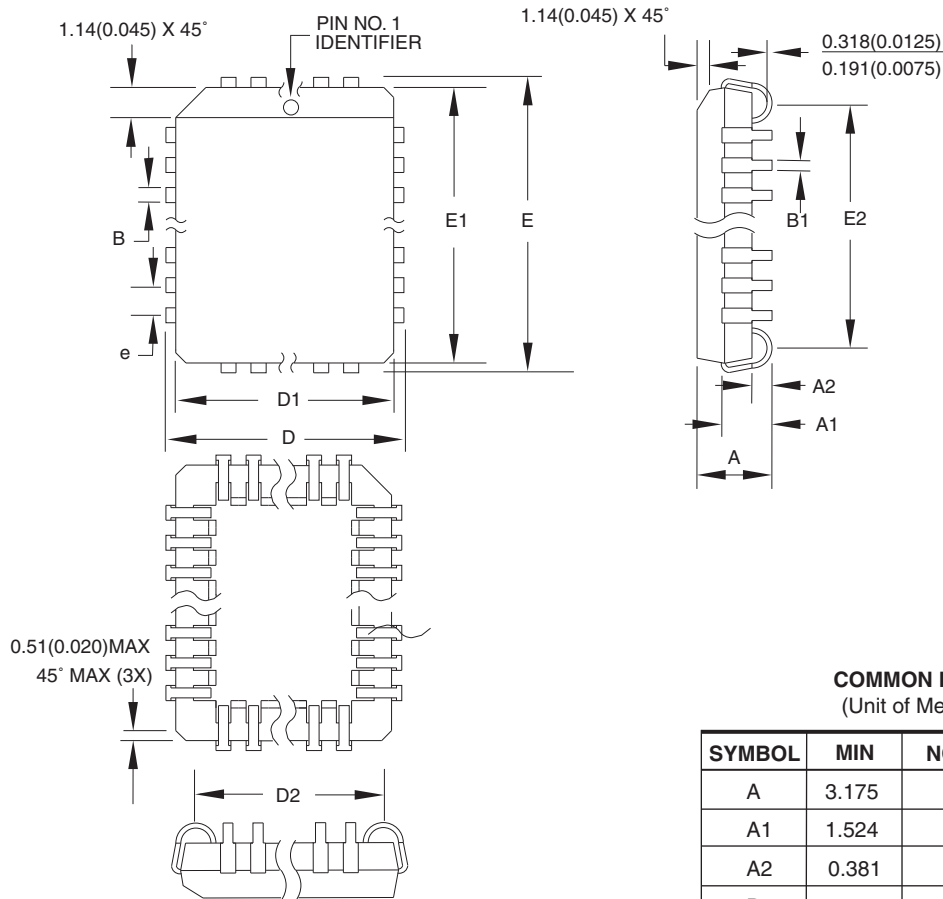
28.1 Green Package Option (Pb/Halide-free)

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	50	03	AT29C512-70JU	32J	Industrial (-40° to 85° C)
			AT29C512-70TU	32T	
90	50	0.3	AT29C512-90JU	32J	
			AT29C512-90TU	32T	

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32T	32-lead, Thin Small Outline Package (TSOP)

29. Packaging Information

29.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.



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TITLE

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

32J

REV.

B